

Amendments to the Specification

Please replace the first paragraph beginning at page 8, line 1, with the following amended paragraph:

Referring next to FIG. 2, translator **10** provides a primary interface **28** for communication with a master on the primary bus **30** and one or more secondary interfaces **32** and **34** (two shown) each for communication with one or more slave devices on secondary buses **36** and **38**. The number of secondary interfaces will typically correspond to the number of secondary buses incorporated in a system. It should be noted that it is the responsibility of the master to pull the one-wire bus to a logic high level. Since the secondary buses **36** and **38** may be isolated from primary bus **28**, the translator must provide a pull-up resistor **40 or 42** for proper operation of the slave devices.

Please replace the first paragraph beginning at page 9, line 1, with the following amended paragraph:

Referring now to FIG. 4, preferably the interface **28, 32, or 34** to each one-wire bus, whether primary **30** or secondary ~~**32**~~**36** or ~~**34**~~**38**, comprises: a receive buffer **16**; and a transistor **64** for pulling the bus low during a transmission. In addition, each secondary bus includes a pull-up resistor **40** or **42**. The CD4050, hex buffer **16** contains six individual receive buffers **16a-f** which will accommodate high voltage programming pulses issued by the master to program EPROM type slave devices. In the preferred embodiment, the external buffer **16** was employed to accommodate such

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Amendment Dated 9/27/04
Reply to Office Action of 06/25/04
Page 3 of 13

a programming voltage. If the inventive translator is used in a system where EPROM programming is not a concern, the receive buffers 16 could be implemented within the FPGA 14.